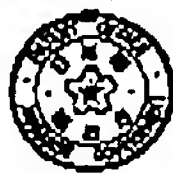


(19)



JAPANESE PATENT OFFICE

Abstract of CITATION 5

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 06112814 A

(43) Date of publication of application: 22.04.94

(51) Int. Cl.

H03L 7/087
H03L 7/06

(21) Application number: 04282343

(22) Date of filing: 28.09.92

(71) Applicant: YAMAHA CORP

(72) Inventor: FUSHIKI TATSURO
FUJIWARA KAZUNOBU

(54) PHASE LOCKED LOOP CIRCUIT

COPYRIGHT: (C)1994,JPO&Japio

(57) Abstract

PURPOSE: To always stably operate without being affected by jitter in a input signal with a wide capture range.

CONSTITUTION: A PLL loop adopting phase comparison is made up of a latch circuit 2 detecting a phase difference between an input signal EFM and a recovered clock signal RCK, a loop filter 4 applying filtering processing to the detected phase difference and a digital oscillator whose frequency is controlled based on the output of the loop filter 4 and outputting a recovered clock signal, and also with frequency comparators 7-14 counting an edge interval of an input signal based on the recovered clock signal and outputting limit values -M, +N for a frequency deviation when it is detected that the count value is at the outside of a prescribed range. When the frequency comparators 7-14 detects it that the count exceeds the prescribed range, the output of the limit value -M is invalidated for a prescribed time. The countup timing and the reset timing of a counter 10 are respectively adjusted by variable delay circuits 8, 9.

